REMARKS/ARGUMENTS

Brief Summary of Status

Claims 1-31 are pending in the application.

Claims 1-31 are rejected.

1. The Examiner asserts:

"Claims 1-31 are provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claim 8 of copending Application No. 10/668,526. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented. Claim 8 of applicants' copending application No. 10/668,526 is so broad that it covers all LDPC decoders that have been or ever will be invented, including that set forth in all the claims of this application." (office action, Part of Paper No./Mail Date 5022005, p. 2)

Remarks

35 U.S.C. § 101

1. The Examiner asserts:

"Claims 1-31 are provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claim 8 of copending Application No. 10/668,526. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented. Claim 8 of applicants' copending application No. 10/668,526 is so broad that it covers all LDPC decoders that have been or ever will be invented, including that set forth in all the claims of this application." (office action, Part of Paper No./Mail Date 5022005, p. 2)

The Applicant respectfully traverses.

The Applicant respectfully points out that claim 8 of the Applicant's co-pending U.S. utility patent application serial no. 10/668,526 (Attorney Docket No. BP3089) was amended and a "Notice of Allowance" been subsequently issued by the Examiner of that case.

The amended and allowed claim 8 of the Applicant's co-pending U.S. utility patent application serial no. 10/668,526 (Attorney Docket No. BP3089) reads as follows:

"8. A decoder, comprising:

a check node update functional block that is operable to update a plurality of edge messages that corresponds to a plurality of edges that communicatively couple a plurality of symbol nodes to a plurality of check nodes within an LDPC (Low Density Parity Check) coded modulation bipartite graph that corresponds to an LDPC code; and

a symbol sequence estimate and symbol node update functional block that is operable to employ the updated plurality of edge messages when making a best estimate of a symbol of a plurality of symbols of a LDPC coded modulation signal."

The Applicant respectfully points out that it is known in the art of decoding LDPC coded signals that the decoding processing is typically performed on a "per bit within an LDPC codeword basis". Generally speaking, prior art LDPC decoding approaches do not operate on a symbol basis, but rather make best estimates of the individual bits of an LDPC codeword.

In other words, when considering prior art decoding approaches of LDPC coded signals, estimates of each individual bit of an LDPC codeword is typically made in the decoding processing. The LDPC bipartite graphs that depict LDPC codes of such prior art approaches typically include (1) bit nodes and (2) check nodes connected by a certain number of edges that interconnect each bit node to selected check nodes.

In other words, these prior art LDPC bipartite graphs are not typically represented using symbol nodes; in contradistinction, they employ bit nodes.

The Applicant's co-pending U.S. utility patent application serial no. 10/668,526 (Attorney Docket No. BP3089) presents a novel approach by which direct decoding can be performed on a symbol basis operates (i.e., without being performed on a bit basis) by using appropriate novel labeling/handling of the relationship between bit nodes and symbol nodes.

Within the Applicant's co-pending U.S. utility patent application serial no. 10/668,526 (Attorney Docket No. BP3089), the Applicant teaches and discloses the distinction and relationships between (1) bit nodes, (2) check nodes, and (3) symbol nodes. In at least FIG. 24A, FIG. 24B, and the corresponding written specification portions of the Applicant's originally filed disclosure of Applicant's co-pending U.S. utility patent application serial no. 10/668,526 (Attorney Docket No. BP3089), the

Applicant shows the distinction between (1) bit nodes, (2) check nodes, and (3) symbol nodes. FIG. 24B of the Applicant's originally filed disclosure shows how the symbol nodes can be directly connected to the check nodes in accordance with certain novel aspects of the Applicant's invention when performing the appropriate novel labeling of the Applicant.

In one such possible embodiment of the Applicant's co-pending U.S. utility patent application serial no. 10/668,526 (Attorney Docket No. BP3089), the edge messages of the FIG. 24B correspond to the edges that communicatively couple the symbol nodes and the check nodes of the LDPC coded modulation bipartite graph. It can be seen that an actual "symbol node" (as disclosed and claimed by the Applicant) actually corresponds to more than one bit; their relationship is handled using the appropriate novel labeling described by the Applicant therein.

Within the Applicant's co-pending U.S. utility patent application serial no. 10/668,526 (Attorney Docket No. BP3089), when using actual "symbol nodes" as disclosed by the Applicant (in at least the Applicant's FIG. 24A and associated written description), it is clear that some edges correspond to more than 1 bit. Because of this, there has to be an appropriate handling of the correspondence between the multiple bits represented by a singular actual "symbol node" and the "bit nodes" to which the "symbol node" corresponds.

The Applicant teaches and discloses therein:

"With respect to the LDPC code bipartite graphs described above, it is noted that the labels of some of the edges correspond to more than 1 bit. For example, for the bits 3, 5, 6, and 7, the edge messages correspond to more than 2 values. Because of this, the common approach of employing LLR (log likelihood ratio) decoding cannot be employed." (specification of Applicant's co-pending U.S. utility patent application serial no. 10/668,526 (Attorney Docket No. BP3089), p. 49, lines 1-3).

During prosecution of the Applicant's co-pending U.S. utility patent application serial no. 10/668,526 (Attorney Docket No. BP3089), the Examiner of that case cited the reference Coker et al. (USPAP 2003/0074626 A1), (hereinafter referred to as "Coker").

Coker employs the relationship between bit nodes and check nodes in accordance with what is typical within the prior art. However, Coker loosely uses the terminology of "symbol nodes" when referring to what actually are "bit nodes" within his disclosure.

The Applicant respectfully points out that the edges of Coker do not communicatively couple between actual "symbol nodes" and "check nodes" at all.

In contradistinction, the edges of Coker actually connect between nodes that actually correspond to individual "bits" of a codeword (i.e., bit nodes) and "check nodes" within an LDPC bipartite graph. The use of terminology of Coker is somewhat ambiguous/unclear, and the Applicant respectfully points out that possible confusion could arise with reference to the "symbol nodes" of Coker, which actually seem to correspond to "bits" (i.e., and not an entire symbol).

Coker teaches and discloses:

"The SPA operates on a bipartite graph associated with a given sparse parity check matrix H having M rows and N columns. This graph has two types of nodes: N symbol nodes corresponding to each bit in a code word x, and M check nodes corresponding to the parity checks $pc_m(x)$, $1 \le m \le M$, represented by the rows of the matrix H. Each symbol node is connected to the check nodes it participates in, and each check node is connected to the symbol nodes it checks. The SPA operates by passing messages between symbol nodes and check nodes. The messages themselves can be a posterioiri probabilities (APP) or log likelihood ratios (LLRs). Typical message parsing schedules alternately compute updates of all symbol nodes and of all check nodes." (Coker, paragraph 0045, lines 6-end of paragraph, emphasis added)

Coker explicitly teaches and discloses that the bipartite graph employed therein has two types of nodes, "symbol nodes" and "check nodes", and specifically the "symbol nodes corresponding to each bit in a code word x". In other words, these "symbol nodes" of Coker do not correspond to more than 1 bit; these "symbol nodes" of Coker are actually only "bit nodes", in accordance with what is employed within the prior art.

Coker explicitly teaches and discloses that the "symbol nodes" correspond to "each bit in a code word". In other words, these "symbol nodes" of Coker are actually "bit nodes", which is the common term typically employed in the art for such nodes wherein each such node of the LDPC bipartite graph corresponds to one bit.

Furthermore, Coker explicitly teaches and discloses that the "SPA operates by passing messages between symbol nodes and check nodes", and since each of the "symbol nodes" of Coker corresponds to only one "bit in a code word", then these "messages" of Coker cannot correspond to edges that communicatively couple actual "check nodes" and "symbol nodes" (as disclosed and claimed by the Applicant in the Applicant's co-pending U.S. utility patent application serial no. 10/668,526 (Attorney Docket No. BP3089)).

Moreover, Coker teaches and discloses:

"A method for decoding Low Density Parity Check (LDPC) codes comprises executing a sum product algorithm to recover a set of information bits from an LDPC code represented as a bipartite graph of symbol nodes and check nodes, the sum product algorithm being responsive to input log likelihood ratios associated with the symbol nodes." (Coker, ABSTRACT, lines 1-6, emphasis added)

"... a set of information bits from an LDPC code represented as a bipartite graph of symbol nodes and check nodes ..." (Coker, claims 1, 4, 6, and 8)

"... a set of information bits from an LDPC code represented as a bipartite graph of symbol nodes and check nodes ..." (Coker, SUMMARY OF THE INVENTION, paragraph 0010)

"... a set of information bits from an LDPC code represented as a bipartite graph of symbol nodes and check nodes ..." (Coker, paragraph 0084)

It seems clear to the Applicant that the LDPC bipartite graph employed by Coker corresponds to "a set of information bits from an LDPC code" and not to symbols "from an LDPC code".

It seems clear to the Applicant that the LDPC bipartite graph employed by Coker includes "check nodes" that should more properly be referred to as "bit nodes" (although Coker refers to them as "symbol nodes").

Throughout Coker, Coker indicates that "a set of information bits", and not the symbols therein, is represented by "an LDPC code represented as a bipartite graph of symbol nodes and check nodes".

This, coupled with the fact that Coker explicitly teaches and discloses the "symbol nodes corresponding to each bit in a code word x", leads the Applicant to the

understanding that the "symbol nodes" of Coker are actually what are typically referred to in the art as "bit nodes".

The Applicant provides this information re: Coker to the Examiner of the instant case to point out that prior art decoding of LDPC coded signals is in fact typically performed on a per bit basis (i.e., just as it is within Coker).

That is to say, with respect to a prior art LDPC bipartite graph, the decoding processing operates to make estimates with respect to each of the individual bit nodes of the LDPC bipartite graph, and each individual bit node corresponds to only one bit of the LDPC codeword.

Within the Applicant's claims, the Applicant respectfully believes that the Applicant claims subject matter that includes decoding processing of LDPC coded signals that includes updating bit node information, updating check node information, and updating bit metrics appropriately for use within the decoding processing.

The Applicant respectfully believes that the Applicant's claimed subject matter, including all limitations thereof, is in fact patentable subject matter over the prior art.

The Applicant respectfully believes that claims 1-31 are in condition for allowance and respectfully requests that they be passed to allowance.

The Examiner is invited to contact the undersigned by telephone or facsimile if the Examiner believes that such a communication would advance the prosecution of the present U.S. utility patent application.

RESPECTFULLY SUBMITTED,

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